*VLSI INTERNSHIP REPORT*

**Semi custom design flow:**

***Designing a counter:***

Verilog code

`timescale 1ns/1ps  
module counter(count,clk,m,rst);  
input clk,rst,m;  
output reg[3:0] count;  
always@(posedge clk or negedge rst)  
begin  
if(!rst)  
count=0;  
else if(m)  
count=count+1;  
else  
count=count-1;  
end  
endmodule

Testbench

`timescale 1ns/1ps  
module counter\_tb();  
reg clk,m,rst;  
wire [3:0]count;  
counter x1(count,m,clk,rst);  
always  
begin  
#5 clk=~clk;  
end  
initial  
begin  
clk=0;  
rst=0;  
#5 rst=1;  
end  
initial  
begin  
m=1;  
#160 m=0;  
$display("time=%t rst=%b clk=%b count=%b", $time,rst,clk,count);  
$finish;  
end  
endmodule

TCL Commands

# liberty file path  
read\_libs /home/install/FOUNDRY/digital/90nm/dig/lib/slow.lib  
# top logic file name  
read\_hdl counter.v  
elaborate  
# sdc file name  
read\_sdc counter\_input.sdc  
# setting effort levels for 3 stages  
set\_db syn\_generic\_effort medium  
set\_db syn\_map\_effort medium  
set\_db syn\_opt\_effort medium  
# synthesis of generic gates  
syn\_generic  
# synthesising for mapping  
syn\_map  
# for optimization  
syn\_opt  
# for sequential circuits  
report\_timing > counter\_timing.repo  
# for combinational circuits  
report\_timing -unconstrained > counter\_timing.repo  
# generating power report  
report\_power > counter\_power.repo  
# generating area report  
report\_area > counter\_area.repo  
# generating netlist from synthesis  
write\_hdl > counter\_netlist.v  
# generating sdc file from synthesis  
write\_sdc > counter\_output.sdc  
# to see the schematic  
gui\_show

Input SDC Commands

create\_clock -name clk -period 2 -waveform {0 1} [get\_ports "clk"]  
set\_clock\_transition -rise 0.1 [get\_clocks "clk"]  
set\_clock\_transition -fall 0.1 [get\_clocks "clk"]  
set\_clock\_uncertainity 0.01 [get\_ports "clk"]  
set\_input\_transition 0.12 [all\_inputs]  
set\_input\_delay -max 0.8 [get\_ports "clk"] -clock [get\_clocks "clk"]  
set\_input\_delay -max 0.8 [get\_ports "m"] -clock [get\_clocks "clk"]  
set\_input\_delay -max 0.8 [get\_ports "rst"] -clock [get\_clocks "clk"]  
set\_output\_delay -max 0.8 [get\_ports "count"] -clock [get\_clocks "clk"]

Area Report

============================================================  
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082\_1  
  Generated on:           Dec 19 2023  10:19:18 am  
  Module:                 counter  
  Operating conditions:   slow (balanced\_tree)  
  Wireload mode:          enclosed  
  Area mode:              timing library  
============================================================  
  
Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload    
--------------------------------------------------------------------------  
counter                  14    130.944     0.000      130.944 <none> (D)    
  (D) = wireload is default in technology library

Power Report

Instance: /counter  
Power Unit: W  
PDB Frames: /stim#0/frame#0  
  -------------------------------------------------------------------------  
    Category         Leakage     Internal    Switching        Total    Row%  
  -------------------------------------------------------------------------  
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
    register     5.83626e-07  4.22522e-05  8.60216e-07  4.36960e-05  87.82%  
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
       logic     1.56684e-07  1.86339e-06  1.24468e-06  3.26476e-06   6.56%  
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
       clock     0.00000e+00  0.00000e+00  2.79450e-06  2.79450e-06   5.62%  
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
  -------------------------------------------------------------------------  
    Subtotal     7.40310e-07  4.41156e-05  4.89940e-06  4.97553e-05 100.00%  
  Percentage           1.49%       88.67%        9.85%      100.00% 100.00%  
  -------------------------------------------------------------------------

Timing report

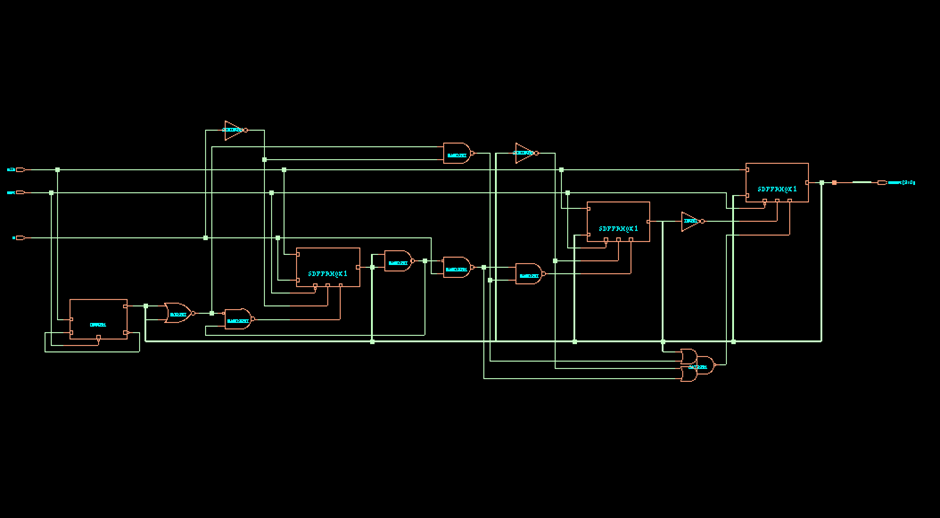
TIMING:

============================================================  
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082\_1  
  Generated on:           Dec 19 2023  10:19:18 am  
  Module:                 counter  
  Operating conditions:   slow (balanced\_tree)  
  Wireload mode:          enclosed  
  Area mode:              timing library  
============================================================  
  
No unconstrained paths found

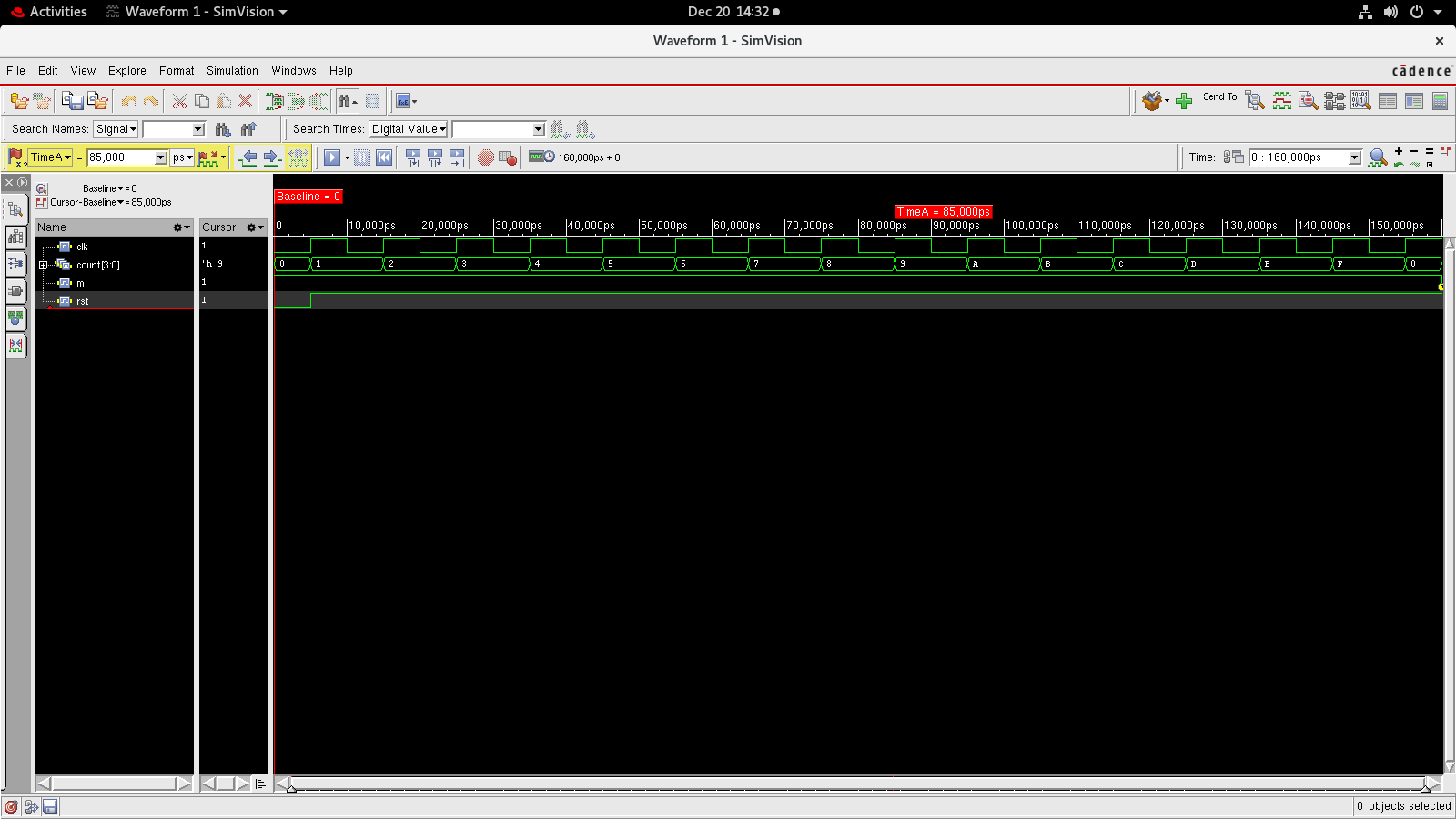
Output SDC file

# ####################################################################  
  
#  Created by Genus(TM) Synthesis Solution 21.14-s082\_1 on Tue Dec 19 10:19:18 IST 2023  
  
# ####################################################################  
  
set sdc\_version 2.0  
  
set\_units -capacitance 1000fF  
set\_units -time 1000ps  
  
# Set the current design  
current\_design counter  
  
create\_clock -name "clk" -period 2.0 -waveform {0.0 1.0} [get\_ports clk]  
set\_clock\_transition 0.1 [get\_clocks clk]  
set\_clock\_gating\_check -setup 0.0  
set\_input\_delay -clock [get\_clocks clk] -add\_delay -max 0.8 [get\_ports m]  
set\_input\_delay -clock [get\_clocks clk] -add\_delay -max 0.8 [get\_ports rst]  
set\_output\_delay -clock [get\_clocks clk] -add\_delay -max 0.8 [get\_ports {count[3]}]  
set\_output\_delay -clock [get\_clocks clk] -add\_delay -max 0.8 [get\_ports {count[2]}]  
set\_output\_delay -clock [get\_clocks clk] -add\_delay -max 0.8 [get\_ports {count[1]}]  
set\_output\_delay -clock [get\_clocks clk] -add\_delay -max 0.8 [get\_ports {count[0]}]  
set\_input\_transition 0.12 [get\_ports clk]  
set\_input\_transition 0.12 [get\_ports m]  
set\_input\_transition 0.12 [get\_ports rst]  
set\_wire\_load\_mode "enclosed"

Counter Schematic circuit



Output Waveforms



GDS File



***Designing a FullAdder***

Verilog code

`timescale 1ns/1ps  
module fulladder(a,b,cin,sum,carry);  
input a,b,cin;  
output sum,carry;  
assign sum=a^b^cin;  
assign carry=(a&b)|(b&cin)|(cin&a);  
endmodule

Testbench

`timescale  1ns/1ps  
module fulladder\_tb();  
reg a,b,cin;  
wire sum, carry;  
fulladder uut(a,b,cin,sum,carry);  
initial begin  
#10 a=0;b=0;cin=0;  
#10 a=0;b=0;cin=1;  
#10 a=0;b=1;cin=0;  
#10 a=0;b=1;cin=1;  
#10 a=1;b=0;cin=0;  
#10 a=1;b=0;cin=1;  
#10 a=1;b=1;cin=0;  
#10 a=1;b=1;cin=1;  
end  
endmodule

TCL Commands

# liberty file path  
read\_libs /home/install/FOUNDRY/digital/90nm/dig/lib/slow.lib  
# top logic file name  
read\_hdl fulladder.v  
elaborate  
# sdc file name  
read\_sdc fulladder\_input.sdc  
# setting effort levels for 3 stages  
set\_db syn\_generic\_effort medium  
set\_db syn\_map\_effort medium  
set\_db syn\_opt\_effort medium  
# synthesis of generic gates  
syn\_generic  
# synthesising for mapping  
syn\_map  
# for optimization  
syn\_opt  
# for sequential circuits  
report\_timing > fulladder\_timing.repo  
# for combinational circuits  
report\_timing -unconstrained > fulladder\_timing.repo  
# generating power report  
report\_power > fulladder\_power.repo  
# generating area report  
report\_area > fulladder\_area.repo  
# generating netlist from synthesis  
write\_hdl > fulladder\_netlist.v  
# generating sdc file from synthesis  
write\_sdc > fulladder\_output.sdc  
# to see the schematic  
gui\_show

Input SDC Commands

set\_input\_transition 0.12 [all\_inputs]  
set\_input\_delay -max 0.8 [get\_ports "a"] -clock [get\_clocks "clk"]  
set\_input\_delay -max 0.8 [get\_ports "b"] -clock [get\_clocks "clk"]  
set\_input\_delay -max 0.8 [get\_ports "cin"] -clock [get\_clocks "clk"]  
set\_output\_delay -max 0.8 [get\_ports "sum"] -clock [get\_clocks "clk"]  
set\_output\_delay -max 0.8 [get\_ports "carry"] -clock [get\_clocks "clk"]

Timing report

============================================================  
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082\_1  
  Generated on:           Dec 19 2023  11:18:43 am  
  Module:                 fulladder  
  Operating conditions:   slow (balanced\_tree)  
  Wireload mode:          enclosed  
  Area mode:              timing library  
============================================================  
  
  
Path 1: UNCONSTRAINED  
     Startpoint: (F) a  
       Endpoint: (R) sum  
  
                   Capture    Launch    
      Drv Adjust:+       0         0    
                                       
       Data Path:-     332              
  
#---------------------------------------------------------------------------------------  
# Timing Point   Flags   Arc   Edge   Cell     Fanout Load Trans Delay Arrival Instance  
#                                                     (fF)  (ps)  (ps)   (ps)  Location  
#---------------------------------------------------------------------------------------  
  a              -       -     F     (arrival)      1  6.2   120     0       0    (-,-)  
  g85\_\_2398/S    -       B->S  R     ADDFXL         1  0.0    48   332     332    (-,-)  
  sum            -       -     R     (port)         -    -     -     0     332    (-,-)  
#---------------------------------------------------------------------------------------

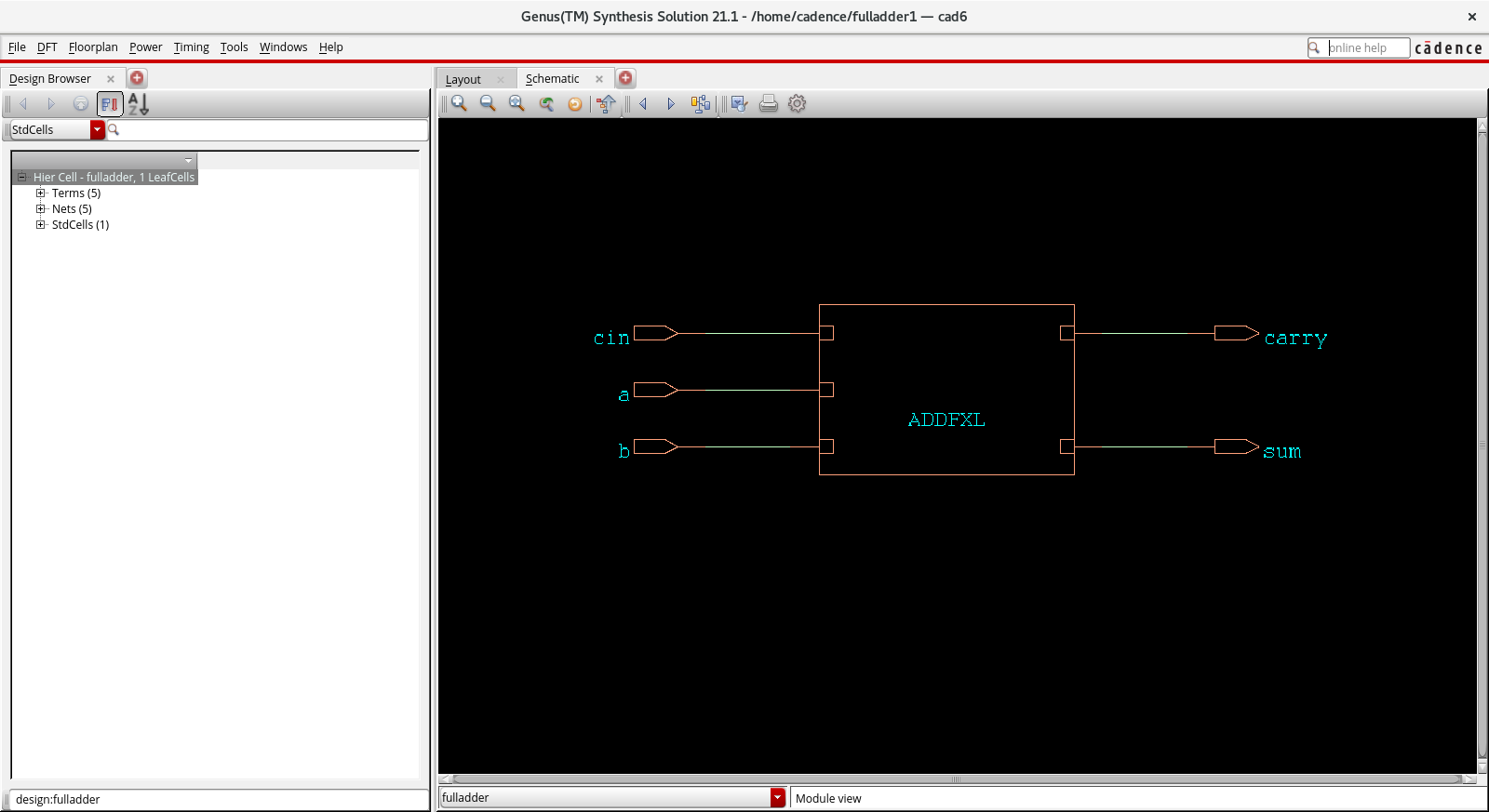
Area Report

============================================================  
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082\_1  
  Generated on:           Dec 19 2023  11:18:43 am  
  Module:                 fulladder  
  Operating conditions:   slow (balanced\_tree)  
  Wireload mode:          enclosed  
  Area mode:              timing library  
============================================================  
  
 Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload    
---------------------------------------------------------------------------  
fulladder                  1     19.679     0.000       19.679 <none> (D)    
  (D) = wireload is default in technology library

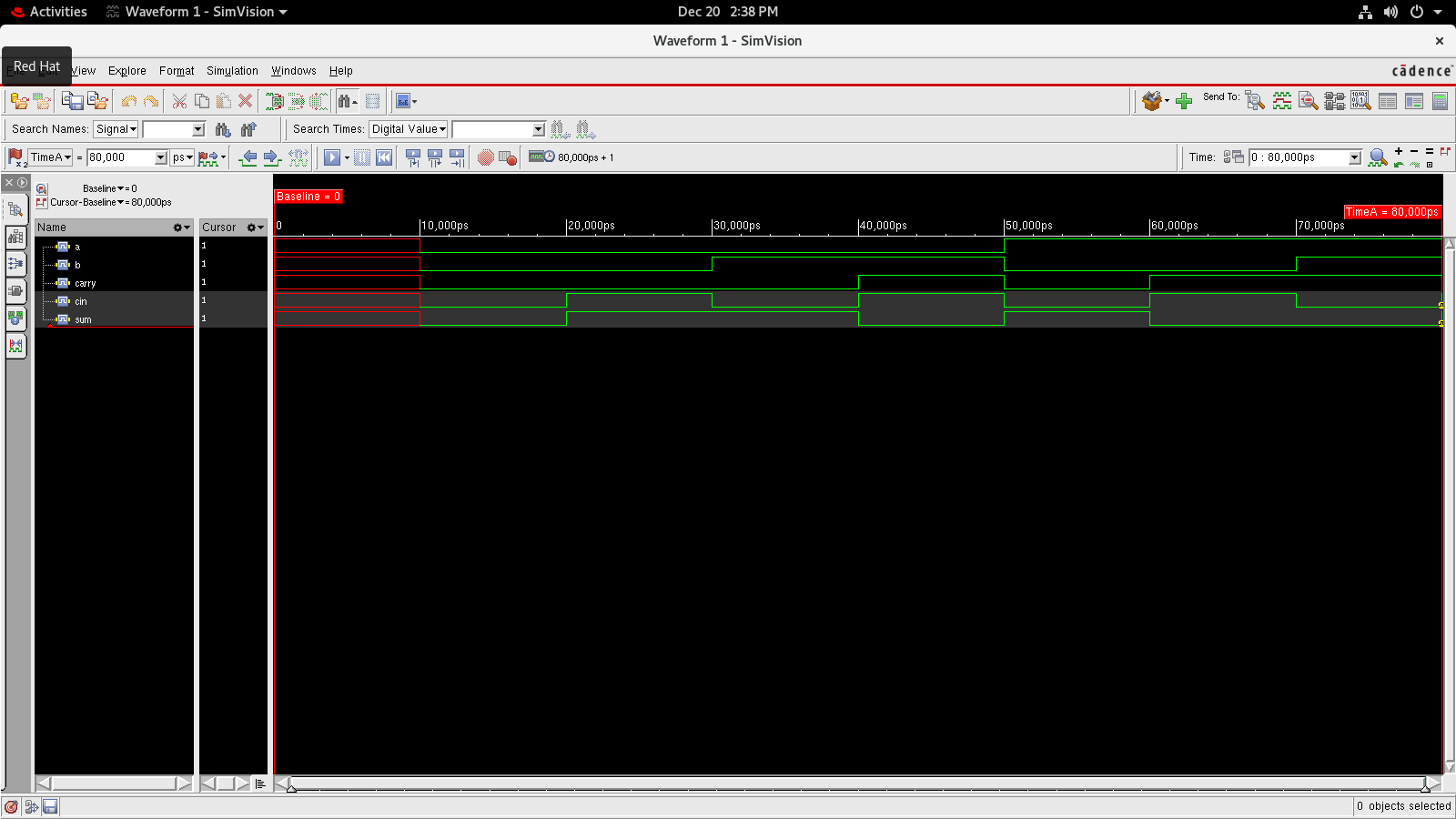
PowerReport

Instance: /fulladder  
Power Unit: W  
PDB Frames: /stim#0/frame#0  
  -------------------------------------------------------------------------  
    Category         Leakage     Internal    Switching        Total    Row%  
  -------------------------------------------------------------------------  
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
    register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
       logic     6.70410e-08  2.07431e-07  1.44180e-07  4.18652e-07 100.00%  
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
       clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
  -------------------------------------------------------------------------  
    Subtotal     6.70410e-08  2.07431e-07  1.44180e-07  4.18652e-07 100.00%  
  Percentage          16.01%       49.55%       34.44%      100.00% 100.00%  
  -------------------------------------------------------------------------

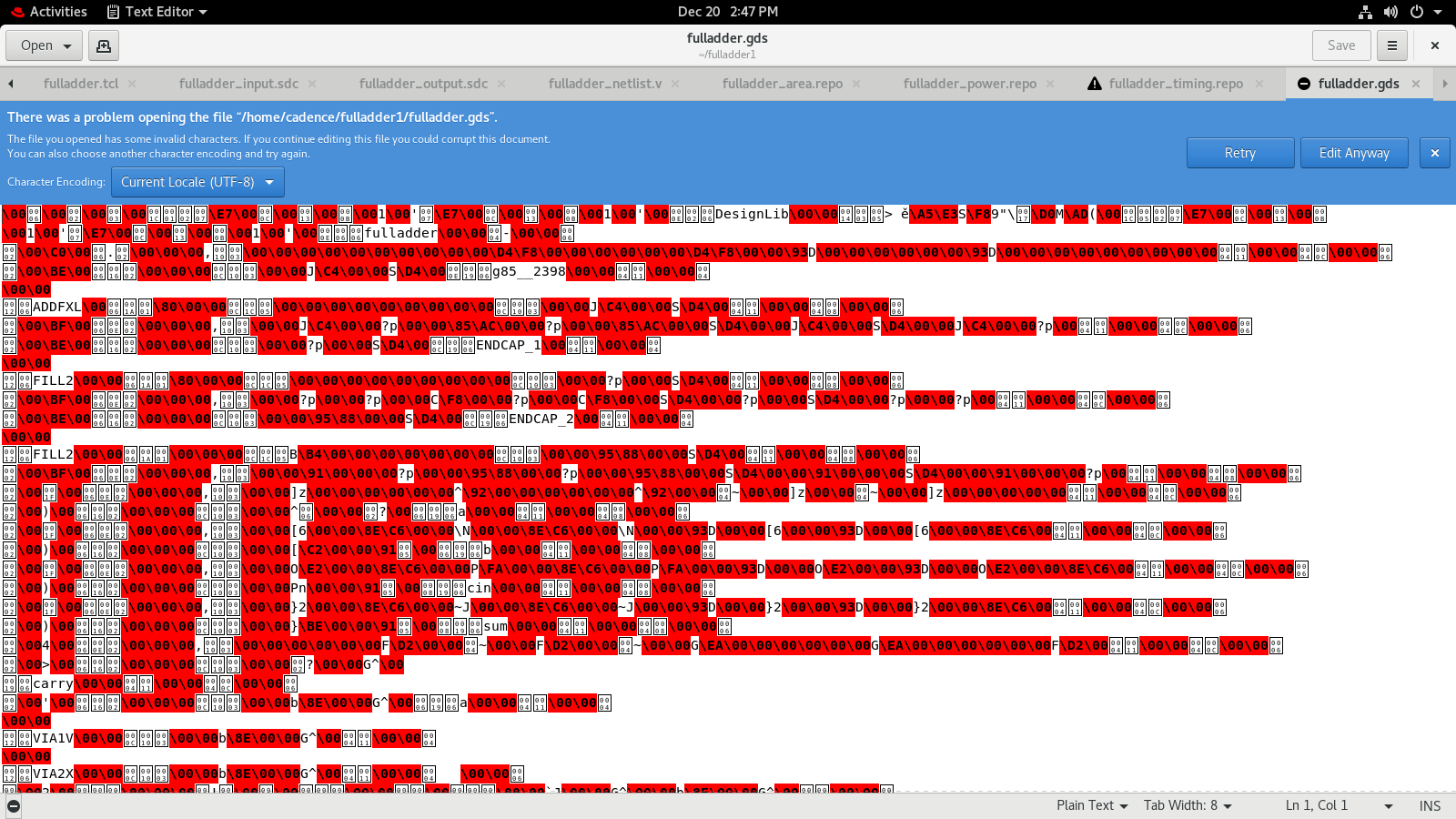
Fulladder Schematic



Output Waveforms



GDS File



***Designing of ALU***

Verilog Code

`timescale 1ns/1ps  
module alu(y,a,b,f,clk,rst);  
input clk,rst;  
input [31:0]a,b;  
input [2:0]f;  
output reg[31:0]y;  
always@(posedge clk or posedge rst)  
begin  
if(rst)  
y<=32'b0;  
else  
begin  
case(f)  
3'b000 : y<=a&b;  
3'b001 : y<=a|b;  
3'b010 : y<= ~(a&b);  
3'b011 : y<=~(a|b);  
3'b100 : y<=a+b;  
3'b101 : y<=a-b;  
3'b110 : y<=a\*b;  
default : y<= 32'bx;  
endcase  
end  
end

endmodule

TestBench Code

`timescale 1ns/1ps  
module alu\_tb();  
reg clk,rst;  
reg [31:0]a,b;  
reg [2:0]f;  
wire[31:0]y;  
alu uut(.y(y),.a(a),.b(b),.f(f),.clk(clk),.rst(rst));  
always  
#5 clk=~clk;  
initial  
begin  
clk=1'b0;  
rst =1'b1;  
end  
initial  begin  
a=32'h00000000;  
b=32'hFFFFFFFF;  
#10 rst =1'b0;  
#10 f=3'b000;  
#10 f=3'b001;  
#10 f=3'b010;  
#10 f=3'b011;  
#10 f=3'b100;  
#10 f=3'b101;  
#10 f=3'b110;  
end  
initial  
  
#100 $finish;  
endmodule

ALU TCL Commands

# liberty file path  
read\_libs /home/install/FOUNDRY/digital/90nm/dig/lib/slow.lib  
# top logic file name  
read\_hdl alu.v  
elaborate  
# sdc file name  
read\_sdc alu\_input.sdc  
# setting effort levels for 3 stages  
set\_db syn\_generic\_effort medium  
set\_db syn\_map\_effort medium  
set\_db syn\_opt\_effort medium  
# synthesis of generic gates  
syn\_generic  
# synthesising for mapping  
syn\_map  
syn\_opt  
# for sequential circuits  
report\_timing > alu\_timing.repo  
# for combinational circuits  
report\_timing -unconstrained > alu\_timing.repo  
# generating power report  
report\_power > alu\_power.repo  
# generating area report  
report\_area > alu\_area.repo  
# generating netlist from synthesis  
write\_hdl > alu\_netlist.v  
# generating sdc file from synthesis  
write\_sdc > alu\_output.sdc  
# to see the schematic  
gui\_show

ALU INPUT SDC

create\_clock -name clk -period 200 -waveform {0 5} [get\_ports "clk"]  
set\_clock\_transition -rise 0.1 [get\_clocks "clk"]  
set\_clock\_transition -fall 0.1 [get\_clocks "clk"]  
set\_clock\_uncertainity 0.01 [get\_ports "clk"]  
set\_input\_delay -max 1.0 -clock clk [all\_inputs]  
set\_output\_delay -max 1.0 -clock clk [all\_outputs]

ALU TIMING REPORT

============================================================  
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082\_1  
  Generated on:           Dec 20 2023  12:31:43 pm  
  Module:                 alu  
  Operating conditions:   slow (balanced\_tree)  
  Wireload mode:          enclosed  
  Area mode:              timing library  
============================================================  
  
No unconstrained paths found

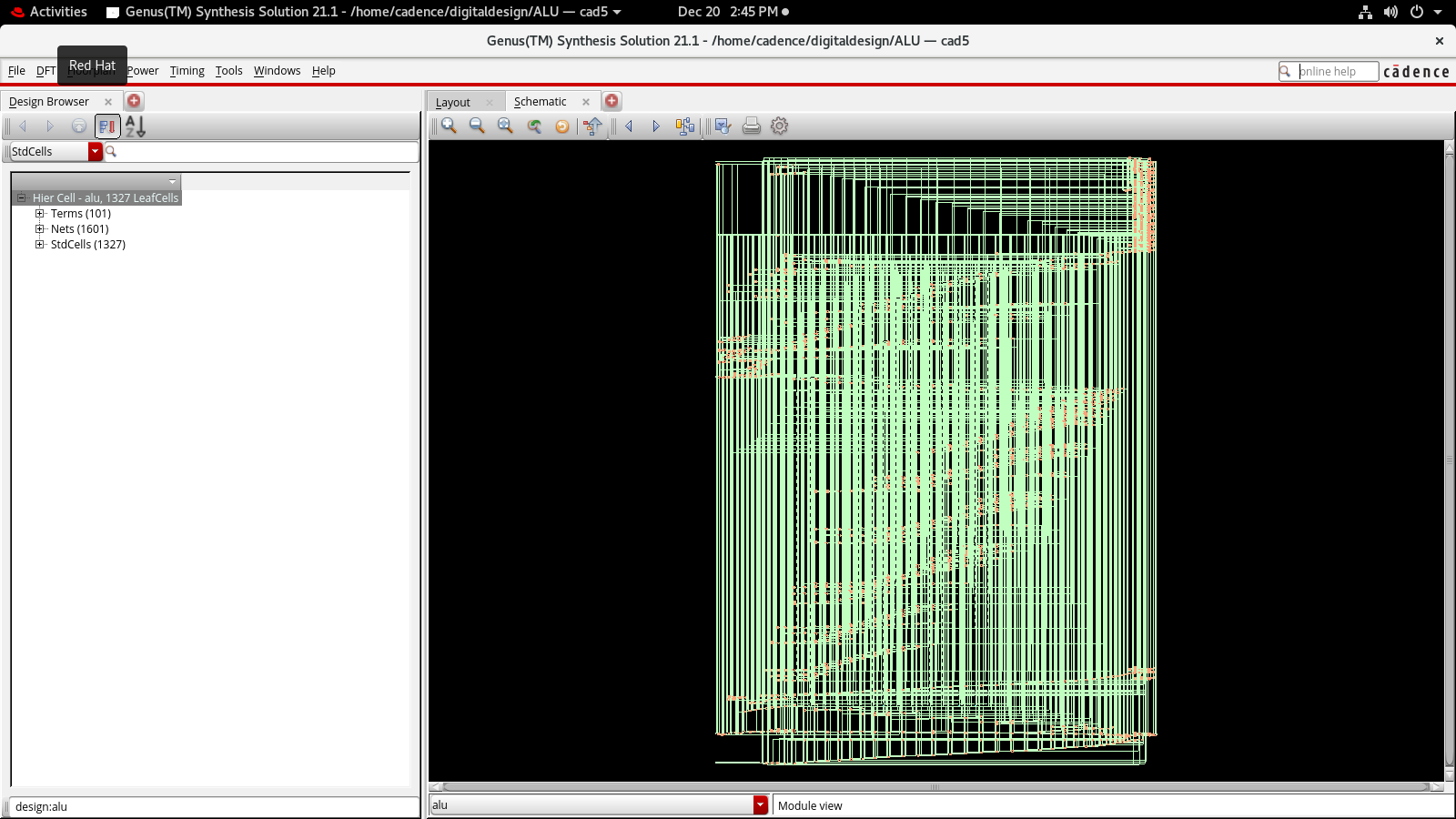
ALU AREA REPORT

============================================================  
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082\_1  
  Generated on:           Dec 20 2023  12:31:43 pm  
  Module:                 alu  
  Operating conditions:   slow (balanced\_tree)  
  Wireload mode:          enclosed  
  Area mode:              timing library  
============================================================  
  
Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload    
--------------------------------------------------------------------------  
alu                    1327  10515.611     0.000    10515.611 <none> (D)    
  (D) = wireload is default in technology library

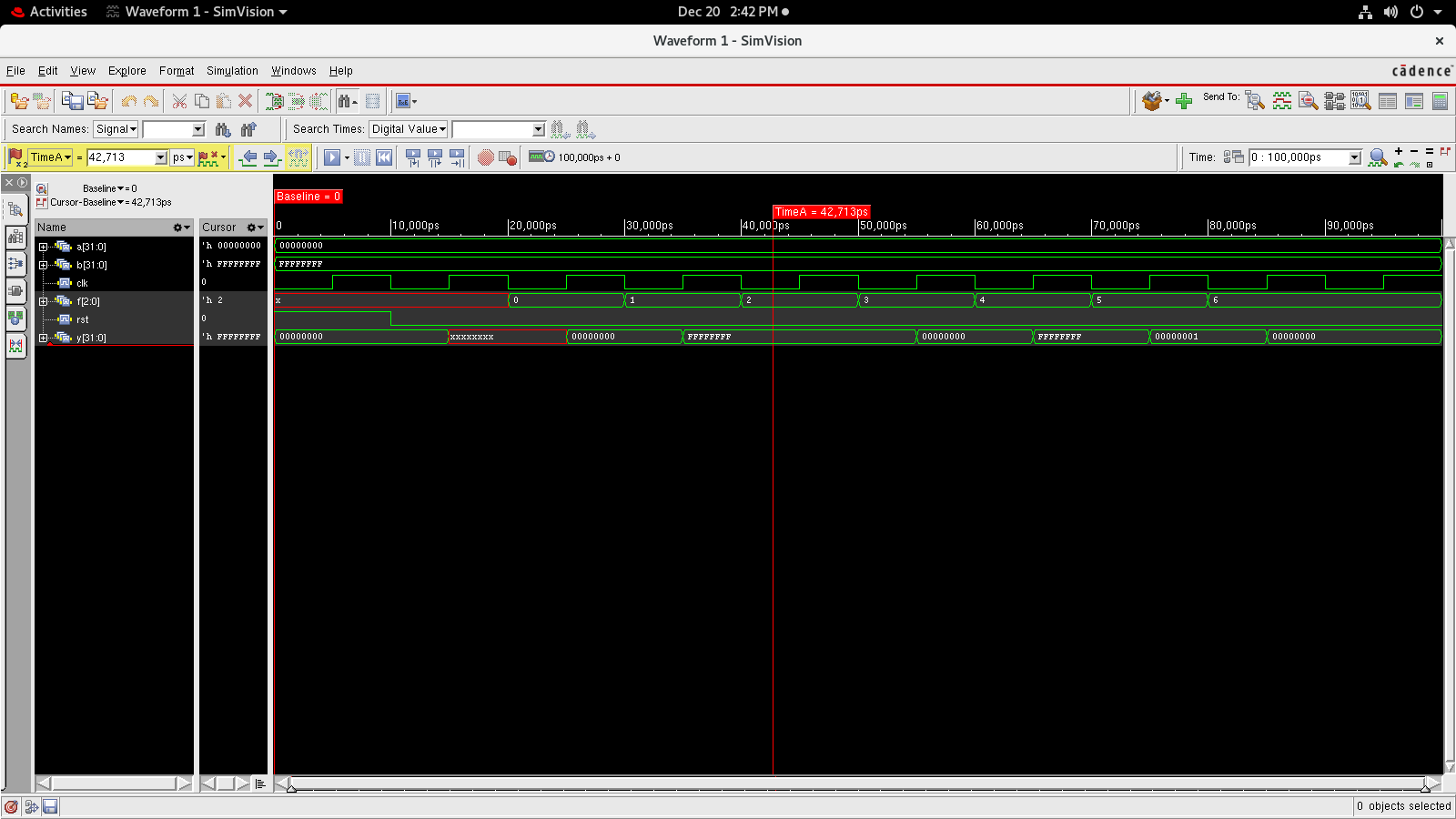
ALU POWER REPORT

Instance: /alu  
Power Unit: W  
PDB Frames: /stim#0/frame#0  
  -------------------------------------------------------------------------  
    Category         Leakage     Internal    Switching        Total    Row%  
  -------------------------------------------------------------------------  
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
    register     3.21446e-06  4.05562e-06  0.00000e+00  7.27008e-06  10.78%  
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
       logic     3.48855e-05  1.59296e-05  9.13499e-06  5.99500e-05  88.90%  
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
       clock     0.00000e+00  0.00000e+00  2.13840e-07  2.13840e-07   0.32%  
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%  
  -------------------------------------------------------------------------  
    Subtotal     3.80999e-05  1.99852e-05  9.34883e-06  6.74339e-05 100.00%  
  Percentage          56.50%       29.64%       13.86%      100.00% 100.00%  
  -------------------------------------------------------------------------

ALU SCHEMATIC DIAGRAM



ALU OUTPUT WAVEFORMS



ALU GDS FILE

